

App. Serial No. 10/566,514  
Docket No. US030253 US2

RECEIVED  
CENTRAL FAX CENTER

MAR 20 2007

Remarks

Claims 1-17 are currently pending in the patent application. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated January 19, 2007 indicated the following: the Abstract is objected to for informalities; claims 1-17 are objected to for informalities; claims 1, 6, 10, 12 and 17 are further objected to; claim 6 stands rejected under 35 U.S.C. § 112(2); claims 1-2, 7-13 and 15-17 stand rejected under 35 U.S.C. § 102(b) over Broxterman *et al.* (US 6,058,467); claim 3 stands rejected under 35 U.S.C. § 103(a) over Broxterman in view of Agrawal *et al.* (US 5,179,716); claim 4 stands rejected under 35 U.S.C. § 103(a) over Broxterman in view of Agrawal, and further in view of Born *et al.* (US 6,131,108); claims 5-6 stand rejected under 35 U.S.C. § 103(a) over Broxterman in view of Born, and further in view of Nukiyama (US 4,926,312); and claim 14 stands rejected under 35 U.S.C. § 103(a) over Broxterman in view of Born.

Regarding the informalities cited in the present Office Action, Applicant has removed the reference nos. formerly provided in the Abstract and Claims, and kindly requests that the objections thereto be withdrawn.

Regarding the objection to a term in claims 1, 6 and 10, Applicant has made amendments that are believed to be consistent with the Examiner's suggestions and submits that these claims objections are also overcome. Applicant requests that the objections be withdrawn.

Applicant respectfully traverses the Section 112(2) rejection of claim 6 for indefinite terminology because the term "clock circuit gated" would be understood by one of skill in the art. More specifically, Applicant submits that in view of the teachings of Applicant's specification one skilled in the art would understand that the phrase "other than clock circuit gated" refers to circuits that do not have setups dependent upon a clock. See, e.g., Applicant's specification at Col. 5, paragraph 34. Notwithstanding, Applicant has amended claim 6 in an effort to facilitate prosecution. Accordingly, Applicant submits that the rejection is improper and requests that it be withdrawn.

Applicant has amended claims 1 and 8 to include limitations generally consistent with the limitations found in one or more of (now cancelled) claims 7, 12 and 13.

App. Serial No. 10/566,514  
Docket No. US030253 US2

Applicant has also cancelled claims 7, 12, 13 and 17 and replaced them with claims 18, 19, 20 and 21.

Applicant submits that the claims 18-21 contain numerous claimed limitations that are not taught or suggested by the cited prior art. For instance, the prior art fails to teach first, second, third and fourth multiplexers that provide the claimed outputs. Accordingly, Applicant requests that the claims be allowed.

Regarding the Section 102(b) rejection of claims 1-2, 8-11 and 15-16 over Broxterman, Applicant submits that the Broxterman reference fails to teach each of the claimed limitations. More specifically, Applicant submits that independent claims 1 and 8 (from which claims 2-6 and 9-11 and 14-16 depend) each contain limitations directed to the operations being performed in a single clock cycle. The Office Action erroneously asserts that the Broxterman reference teaches correspondence to the claimed read operation occurring in a single clock cycle. It appears that the Office Action is confusing a single memory operation with a single clock cycle. More specifically, the cited portion of the Broxterman reference, Col. 5, lines 16-18, discusses reducing the number RAM reads from two to one read. Applicant respectfully submits that RAM read is not equivalent to a clock cycle. Moreover, the circuit of the Broxterman reference is taught to use four clock cycles. See, Col. 4, lines 41-56. Thus, because each element of the claimed invention is not taught by the Broxterman reference, the rejections cannot stand. Applicant respectfully requests that the rejections be removed.

The Section 103(a) rejection of claims 3-6 and 14, each of which primarily relies on Broxterman '467, cannot stand for at least the reasons set forth above, and as discussed in further detail below. Applicant respectfully requests that the rejections be withdrawn.

With particular regard to claim 3, Applicant respectfully traverses the rejection. Applicant submits that the Office Action has failed to provide adequate motivation or suggestion to perform the asserted modifications. More specifically, Applicant submits that the Office Action erroneously asserts that the proposed modification would function to provide flexible I/O to the circuit of the Broxterman reference. While the Office Action provides little explanation regarding how such modifications are being asserted, Applicant submits that simply adding the SMUX 304 to the Broxterman circuit would not

App. Serial No. 10/566,514  
Docket No. US030253 US2

produce meaningful results. Accordingly, it is unclear how the Office Action asserts that the SMUX 304 of the Agrawal reference could modify the circuit of the Broxterman reference and provide the asserted functionality. Moreover, the Office Action admits that necessary modifications would be required, but fails to provide teachings that show or suggest any such modifications. The Office Action also fails to provide an explanation of what the modifications would be. Applicant submits that even assuming *arguendo* that it would be possible for the SMUX 304 of the Agrawal reference to provide flexible I/O to the asserted Broxterman circuit; such modifications would require fundamental changes to the functionality of the Broxterman circuit. Should the Examiner wish to clarify necessary aspects of the asserted modifications and the motivation or suggestion to make such modifications, Applicant respectfully requests an opportunity to respond. For at least the aforementioned reasons, Applicant submits that the Office Action has not shown the proper motivation or suggestion to combine the references and requests that the rejection be withdrawn.

With regard to claims 4, 6 and 14, Applicant respectfully traverses the rejections for failing to provide the requisite motivation or suggestion to combine. The Office Action erroneously asserts that one skilled in the art would be motivated to make the asserted modification in order to simplify the circuit design to generate multi bit output. Applicant respectfully submits that such an assertion is illogical because the proposed modifications would not simplify the circuit design to generate multi bit output. More specifically, Applicant does not recognize any portion of the asserted Broxterman reference that would be simplified by the addition of the asserted portions of the Born reference. For example, Applicant notes that the asserted multiplexer of the Born reference receives 48 bits as inputs and provides a 16 bit output for use by a ALU that accepts only 16 bits. In contrast, the Broxterman reference is generally directed to 8-bit controllers and the largest bus in the asserted Broxterman circuit provides a mere 8 bits of data. Accordingly, Applicant submits that the Office Action's proposed modification would likely *complicate* the Broxterman circuit. Thus, the Office Action's asserted motivation or suggestion to implement the proposed modification using the multiplexer of the Born reference is not present.

App. Serial No. 10/566,514  
Docket No. US030253 US2

With particular regard to claim 14, Applicant respectfully traverses the rejection for failing to provide the requisite motivation. The Office Action erroneously asserts that one skilled in the art would be motivated to make the asserted modification in order to simplify the circuit design to generate multi bit output. Applicant respectfully submits that such an assertion is illogical because the proposed modification is directed to write back target addresses and not directly related to multi bit output. Accordingly, Applicant submits that the proposed modification would not simplify the circuit design to generate multi bit output.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, at (408) 474-9063.

*Please direct all correspondence to:*

Corporate Patent Counsel  
NXP Intellectual Property & Standards  
1109 McKay Drive; Mail Stop SJ41  
San Jose, CA 95131

By:   
Name: Robert J. Crawford  
Reg. No.: 32,122  
(NXPS.223PA)

CUSTOMER NO. 65913